The magnitude of DC current component is proportional to the active power demanded by the load plus power losses at steady state. The DC current component is controlled using an inner current loop. This loop minimizes the error between the reference and the actual DC current component and gives a compensating signal of

$$v^*_{dtx} = k_{pi}(i^*_{xd} - i_{xd}) + k_{ii}\int (i^*_{xd} - i_{xd})dt \tag{3.4}$$

where k_{pi} and k_{ii} are the proportional and integral gain of current control loop, respectively.

The actual DC-bus current is estimated from the measured arm currents and is given by

$$i_{xd} = \frac{\mathbf{i_{xu}} + \mathbf{i_{xl}}}{6} \tag{3.5}$$

where $\mathbf{i_{xu}} \in \{i_{au}, i_{bu}, i_{cu}\}$ and $\mathbf{i_{xl}} \in \{i_{al}, i_{bl}, i_{cl}\}$. The compensating signal v^*_{dtx} is used to correct the submodule duty cycles, thereby, the average voltage of each leg is maintained constant.

3.3.2 Voltage Balance Strategy

Voltage balancing among the submodules is a vital factor for the reliable operation of modular multilevel converters. The basic principle of voltage balancing approach is to control the charging and discharging of submodule capacitors on the basis of the arm current direction and the instantaneous value of capacitors voltage. For the positive direction of the current, capacitors with the lowest voltage are inserted in the arm to achieve voltage balancing and vice versa. The voltage balancing can be achieved at the control stage by using a closed-loop PI-controller to control each submodule capacitor voltage independently. The output of the PI-controller is added to the modulation signal of the corresponding submodule. This approach is suitable to implement with PSC-PWM only. On the other hand, the voltage balancing can be achieved at a modulation stage by using logical function-based algorithm. In this approach, all the submodules in each arm are controlled together. Hence, this approach is suitable to implement with any PWM scheme. The flow chart of a simple voltage balance strategy based on logical functions is shown in Figure 3.4(a). The implementation of balancing strategy involves the following steps [9]:

- Measure the SM capacitor voltages ($v^x_{Cyh} \in \{v^x_{Cy1}, v^x_{Cy2}, \ldots, v^x_{CyN}\}$) in each arm, and feed their magnitude value to the comparison logic as shown in Figure 3.4(b).
- In comparison logic, each capacitor voltage is compared with other capacitor voltages. The output of each comparator is added together to obtain an index number (VI_h). The highest index number is assigned to the submodule with the lowest capacitor voltage and vice versa.
- Measure the arm current (i_{xy}) and determine its direction (A_d). For positive direction $A_d = 1$, and for negative direction $A_d = 0$ is assigned.

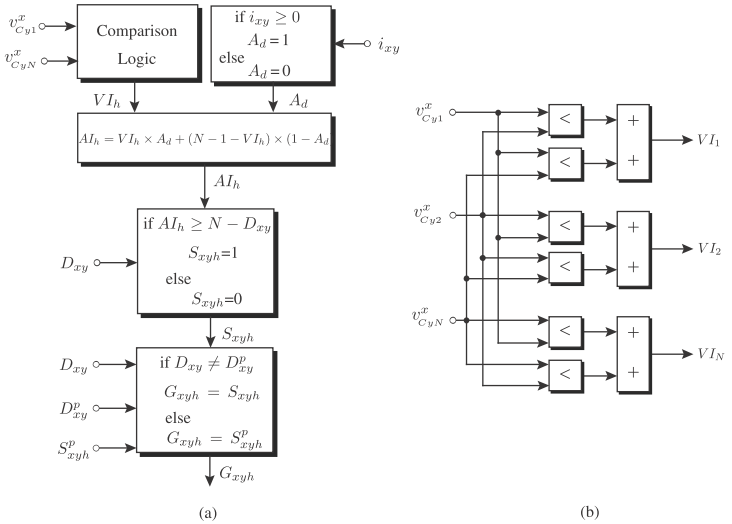

Figure 3.4 Voltage balance strategy: (a) flow chart of balancing strategy, and (b) comparison logic.

- Arrange the submodule index numbers in either ascending or descending order based on the direction of arm current. A simple mathematical expression is presented below to arrange the submodule index numbers.

$$AI_h = VI_h \times A_d + (N - 1 - VI_h) \times (1 - A_d) \tag{3.6}$$

  Equation (3.6) rearranges the submodule index numbers based on the arm current direction. Thereby, the submodules with lowest capacitor voltage are inserted in the arm for the positive current direction and are charged (increasing their voltage). Similarly, the submodules with highest capacitor voltage are inserted in the arm for the negative current direction and are discharged (reducing their voltage).

- Obtain the required number of inserted submodules (D_{xy}) from the modulation stage.

- Compare the actual index number of each submodule (AI_h) with the reference index number ($N - D_{xy}$) to generate the `INSERT = 1` or `BYPASS = 0` states for each submodule (S_{xyh}).

- The inserted number of submodules in the present control cycle (D_{xy}) is compared with the previous control cycle D^p_{xy}. The difference in D_{xy} and D^p_{xy} allows to apply the new gating signals (i.e., $G_{xyh} = S_{xyh}$) or the gating signals in previous